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BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610

EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,173	KIM ET AL.	
	Examiner	Art Unit	
	Tom V. Sheng	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2004 and 22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,22-30,33,34,44,46-49,52,53,63,65 and 66* is/are rejected.

7)☒ Claim(s) *19-21,31,32,35-43,45,50,51,54-62 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/23/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the left and right pixel regions and electrodes and correspondence with associated gate and data lines (cited at least in claims 1-6), the switching parts of the first and second gate lines (cited at least in claim 1), and the gate drive IC with respective terminal and selection part (cited at least in claim 9) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, lines 7-8, it is unclear as to the scope of "by switching parts of the first and second gate lines." The limitation could mean either using switching-parts to alternatively drive the first and second gate lines or could mean the switching of parts of the first and second gate lines. Claims 2-16 are dependent on claim 1.

As for claims 11 and 12, claim 11 cites that the selection block is 10.85 us and claim 12 cites for 21.7 us. Please clarify the meaning of selection block and which time interval is the applicant intended.

As for clams 13 and 14, claim 13 cites the use of 6 gate drive ICs while claim 14 cites the use of 3 gate drive ICs. Please clarify which is the intended claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US 6,825,822 B2).

As for claim 1, Lee teaches a liquid crystal display device (LCD panel; fig. 3) comprising:

a plurality of pairs of gate lines (gate lines Sm and Sm+1 as shown) including first and second gate lines adjacent to each other (gate lines Sm and Sm+1 are adjacent to each other);

a plurality of data lines perpendicular to the first and second gate lines (data line Dn is perpendicular to gate lines Sm and Sm+1 as shown), thereby defining a plurality of left and right side pixel regions (right pixel RP(m,n) and left pixel LP(m,n) are set on the right and left sides of the data line Dn); and

left and right side pixel electrodes (inherently the ends of capacitors C1 and C2 not connected to ground; liquid crystal is capacitive by nature), respectively formed in the left and right side pixel regions (C1 is associated with left pixel LP and C2 is associated with the right pixel RP; column 2, lines 13-40), and selectively driven by switching parts of the first and second gate lines (the left pixel LP is turned on by selectively turning on TFTs M11 and M12 by enabling both gate lines Sm and Sm+1

while the right pixel RP is turned on by selectively turning on TFT M2 by enabling only gate line Sm; column 2, line 41 through column 3, line 7).

As for claim 8, it is inherent that the number of outputs of the source drive ICs is dependent on the number of colors per pixel (i.e. the number of color subpixels in each pixel) because usually each color is controlled by one data line. Further, since two adjacent pixels share a data line, the number of outputs needed is correspondingly reduced in half. As a result of above two features, naturally the number of source driver ICs would correspond to the claimed limitation.

6. Claims 1, 2, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hebiguchi et al. (US 6,583,777 B2), hereinafter Hebiguchi.

As for claim 1, Hebiguchi teaches a liquid crystal display device (fig. 1) comprising:

a plurality of pairs of gate lines (pairs of first gate line GAi and second gate line GBi; column 9, lines 1-4);

a plurality of data lines perpendicular to the first and second gate lines (data lines Dj-2, Dj, and Dj+2; column 8, lines 60-67), thereby defining a plurality of left and right side pixel regions (left pixel PX (i, j) and right pixel PX (i, j+1) as shown coupled to data line Dj); and

left and right side pixel electrodes (the end of respective capacitors not connected to the common potential as shown), respectively formed in the left and right side pixel regions (as shown), and selectively driven by switching parts of the first and

second gate lines (the specification talks about the driving of pixels between data lines, and the same principle applies to driving of the two adjacent pixels PX (i, j) and PX (i, j+1) coupled to data line Dj; that is, right pixel PX (i, j) is driven/enabled by data line GAi and left pixel PX (i, ,j+1) is driven/enabled by gate line GBi alternately).

As for claim 2, the driving of the two adjacent pixels PX (i, j) and PX (i, j+1) coupled to data line Dj; that is, right pixel PX (i, j) is driven/enabled by data line GAi and left pixel PX (i, ,j+1) is driven/enabled by gate line GBi alternately, corresponds to claimed respective driving of left and right pixel electrodes connected with the same data line.

As for claim 8, it is inherent that the number of outputs of the source drive ICs is dependent on the number of colors per pixel (i.e. the number of color subpixels in each pixel) because usually each color is controlled by one data line. Further, since two adjacent pixels share a data line, the number of outputs needed is correspondingly reduced in half. As a result of above two features, naturally the number of source driver ICs would correspond to the claimed limitation.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 28-30, 33, 34, 44, 46-49, 52, 53, 63, 65 and 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hebiguchi.

As for claim 3, Hebiguchi, in the embodiment of fig. 1, does not teach overlapping of any pixel electrode with a preceding or corresponding pair of gate lines. On the other hand, in the embodiment of fig. 11, Hebiguchi teaches overlapping of a pixel electrode with either a corresponding pair of gate lines or a succeeding pair of gate lines (column 13, lines 43-61). One of ordinary skill in the art would recognize the benefit of building up a capacitance so as to further retain a particular of display with a corresponding pixel. Therefore, it would have been obvious to provide at least the overlapping of a pixel electrode with a corresponding pair of gate lines, as claimed, so as to retain the state of display by holding longer the charge of the pixel via an increase in capacitance.

As for claims 28, 30, 47 and 49, the rejection of claim 3 applies. Additionally, as shown in fig. 1 or 11, there is no overlap between any two pixel regions. Further, it would have obvious to overlap more than one gate line in order to provide for more charge storage by having more capacitance. Moreover, the specification or claim does not provide for any novel advantage for overlapping exactly two gate lines.

As for claims 29 and 48, as shown in fig. 11, any two adjacent pixels for each data line have their respective pixel electrodes overlapping different gate lines.

As for claims 33 and 52, each set of gate lines (fig. 1; for example, GAi and GBi) if formed of exactly two gate lines.

As for claims 34 and 53, storage capacitor Cs (fig. 11) is formed by an overlap between a pixel electrode and a gate line.

As for claims 44 and 63, Hebiguchi teaches that his display requires only half of the usual number of data lines but twice the number gate lines (because of the use of one data line and two gate lines for two adjacent pixel; column 10, lines 48-65). In this regard, the number of drive ICs required corresponds to claimed limitation. For example, for XGA format of 1024 x 768, the number of data lines required for color display would be 1024 x 3 / 2 or 1536 and the number of drive ICs required would be 1536 / n (n as number of outputs per drive IC).

As for claims 46 and 65, since the number of data lines are halved and the number of gate lines are doubled, of course the number of source drive ICs would be smaller than the number of gate drive ICs, provided that the number of outputs per IC on both are about the same.

Claim 66 is rejected per rejections of claims 47 and 65.

9. Claims 9-18 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebiguchi as applied to claim 1 above, and further in view of Hashimoto et al. (US 6,072,457), hereinafter Hashimoto.

As for claims 9, 17, 18 and 23, Hebiguchi teaches all the limitations regarding the plurality of pair of gate lines, plurality of data lines defining a plurality of left and right side pixel regions, and corresponding left and right side pixel electrodes selectively driven by switching parts of the first and second gate lines, as analyzed in the rejection of claim 1.

However, Hebiguchi does not teach a gate drive IC supplying a scanning signal to one of the pairs of gate lines, and a selection part time-dividing the scanning signal by selectively applying the time-divided scanning signal to the first and second gate line of the pair of gate lines.

Hashimoto teaches an interlace circuit 60 (fig. 3; column 6, lines 11-26). Hashimoto's vertical scan pulses V1... and vertical selection pulses ΦGo, ΦGe correspond to claimed scanning signals and time-dividing (signals) respectively. Thus, Hashimoto teaches a gate drive IC (inherent) supplying a scanning signal (V1, etc.) to one of the pairs of gate lines (L1 and L2), and a selection part (note the selection transistors bounded by V1... and ΦGo, ΦGe) time-dividing (interlaced within each scan) the scanning signal by selectively applying the time-divided scanning signal to the first and second gate line of the pair of gate lines (fig. 5B; as V1 is active, corresponding active selection pulse ΦGo, ΦGe would make L1 and L2 active in sequential/time-divided manner; column 7, lines 1-32). This has the benefit of being able to using only k horizontal scans to scan m rows or pixels (column 3, lines 37-60).

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate Hashimoto's interlacing into Hebiguchi's display, as it allows interlacing from k scanning signals to m rows of scan, and reduces the scan IC size consequently.

As for claim 22, it is inherent that the number of outputs of the source drive ICs is dependent on the number of colors per pixel (i.e. the number of color subpixels in each pixel) because usually each color is controlled by one data line. Further, since two adjacent pixels share a data line, the number of outputs needed is correspondingly

reduced in half. As a result of above two features, naturally the number of source driver ICs would correspond to the claimed limitation.

As for claims 10 and 24, Hebiguchi does not specifically teach an XGA class display. On the other hand, Hebiguchi's display is equally suitable to be made for XGA display or any other class of display resolution. Moreover, Hebiguchi clearly teaches his display requires only half of the usual data lines but twice the gate lines (column 10, lines 48-65). In the case of XGA display, the format is 1024x768, thus the number of data lines required for display would be 1024 x 3 / 2 or 1536, and the number of gate lines required would be 768 x 2 or 1536.

As for claims 11, 12 and 25, the selection time of each gate line is 1 / 60 / 1536 or 10.85 usec and 2 x 10.85 usec or 21.7 usec is used for each scan signal.

As for claims 13 and 14, for a 256 pin gate drive IC, the number of ICs required would be 1536 / 256 / 2 or 3.

As for claims 15 and 26, for a 384 pin source drive IC, the number of ICs required would be 1536 / 384 or 4.

As for claims 16 and 27, since the number of data lines is halved and the number of gate lines is doubled, the number of source drive ICs would naturally be smaller than the number of gate drive ICs, provided that the number of output terminals for the two types of IC are about the same.

Allowable Subject Matter

10. Claims 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 31, 32, 35-43, 45, 50, 51, 54-62, 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches the limitations, "wherein at least one pixel electrode of adjacent pixel electrodes overlaps at least two gate lines of one of the sets of adjacent gate lines" of claims 31 and 50, "wherein at least one pixel electrode of adjacent pixel electrodes overlaps one of the gate lines of a first set of the sets of adjacent gate lines and one of the gate lines of a second set of the sets of adjacent gate lines" of claims 32 and 51, "a gate drive IC having a scanning signal output terminal corresponding to at least one of the sets of adjacent gate lines, the scanning signal output terminal supplying a scanning signal; and a selection part time-dividing the scanning signal output from the gate drive IC and selectively applying the time-divided scanning signal to the gate lines of the one of the sets of adjacent gate lines" of claims 35 and 54, "a plurality of gate drive ICs, each gate drive IC having a plurality of scanning signal output terminals, each scanning signal output terminal corresponding to a particular set of the sets of the gate lines and supplying a scanning signal to the particular set; and a plurality of selection parts, each selection part time-dividing the scanning signal output from a particular scanning signal output terminal of one of the

gate drive ICs and selectively applying the time-divided scanning signal to one of the gate lines of the particular set" of claims 45 and 64.

13. Claims 4-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V. Sheng whose telephone number is (571) 272-7684. The examiner can normally be reached on 9:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tom Sheng
August 30, 2006

AMR A. AWAD
PRIMARY EXAMINER